## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Maurice B. STEINMAN

et al.

**Anticipated** 

Group Art Unit: 2189

Serial No.: Not Yet Assigned

Anticipated

Filed:

Concurrently Herewith

Examiner:

Tim T. Vo

For:

Computer Architecture And System For Efficient

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Docket No.:

200301842-2

Date: February 17, 2004

**Bi-Directional Bus** 

## PRELIMINARY STATEMENT

Mail Stop Patent Application Commissioner for Patents PO Box 1450 Alexandria, VA 22313-1450

Sir:

At least some of the claims in this continuation application (claim 1 for instance) are carried over from the parent case (Serial No. 09/652,323). As Applicants previously explained, claim 1 addresses reducing "the number of transitions between read transactions and write transactions." In the Examiner's Final Office Action dated June 2, 2003, the Examiner stated:

In response to newly amended feature 'to reduce number of transitions between read transactions and write transaction' does not change scope of claims because once a read and a write transaction is being selected to read or write in a read and a write queue would reduce number of transactions in the queues. For example if there were N of transaction in the read and write queue. When a transaction is being selected to read or write the N of transaction would become N-1 of transactions. For this reason the rejection from previous office sustained.

The Examiner appears to have misread claim 1. Claim 1 refers to reducing "transitions" between reads and writes, while the Examiner refers to reducing the number of "transactions." The Examiner's point appears to be that issuing a transaction from a queue naturally reduces the number of transactions in that queue. Agreed. Claim 1, however, refers to reducing transitions between read

transactions and write transactions. The Examiner is respectfully requested to consider this issue when revisiting the patentability of claim 1.

Respectfully submitted,

Jonathan M. Harris

PTØ Reg. No. 44,144

CÓNLEY ROSE, P.C. (713) 238-8000 (Phone)

(713) 238-8008 (Fax)

ATTORNEY FOR APPLICANTS

HEWLETT-PACKARD COMPANY Intellectual Property Administration Legal Dept., M/S 35 P.O. Box 272400 Fort Collins, CO 80527-2400